## IN THE CLAIMS

Please amend claims 1 and 32, and cancel claims 3, 33 and 38 without prejudice or disclaimer as follows

1. (currently amended) A power amplifier circuit arrangement, comprising:

a first circuit element which receives an input signal, said first circuit element producing an in-phase signal and an out-of-phase signal;

a first power amplifier which receives and amplifies said in-phase signal;

a second power amplifier which receives and amplifies said out-of-phase signal;

a first switch which alternately connects an isolated port of said first circuit element between ground and a bypass path;

a second circuit element which receives and combines said amplified in-phase signal and said amplified out-of-phase signal; [and]

a second switch which alternately connects an isolated port of said second circuit element to ground or said bypass path;

a band-pass filter which receives a signal and outputs a band-passed signal; and

a driver stage which receives said band-passed signal and produces said input signal to be transmitted to said first circuit element.

2. The power amplifier circuit arrangement of claim 1, wherein when said first amplifier and said second amplifier are powered down, said first and second switches connect said isolated ports of said first and second circuit elements via said bypass path in order to bypass said first and second amplifiers.

3. (cancel)

4. The power amplifier circuit of claim 3, wherein a bias and control circuit biases said driver stage, said first power amplifier, and said second power amplifier, said bias and control circuit also controlling said first and second switches.

5. The power amplifier circuit of claim 1, wherein said first circuit element is a coupler and said second circuit element is a coupler.

6. The power amplifier circuit of claim 1, wherein said first circuit element, said first power amplifier, said second power amplifier, said second circuit element, and said first switch are integrated into a single power amplifier package.

7. The power amplifier of claim 1, further comprising a first terminating resistor connected to a pole of said first switch, and a second terminating resistor connected to a pole of said second switch.

8. The power amplifier of claim 7, wherein said first circuit element, said first power amplifier, and said second power amplifier, said second circuit element, said first switch and said first terminating resistor are integrated into a single power amplifier package.

9. The power amplifier of claim 3, wherein said first circuit element, said first power amplifier, and said second power amplifier, said first switch and said first terminating resistor are integrated into a single package.

10. The power amplifier of claim 1, wherein said first circuit element is a branch-line coupler, and said second circuit element is a branch-line coupler.

11. The power amplifier of claim 8, wherein said second switch and said second terminating resistor are also integrated into said single package.

12. The power amplifier of claim 9, wherein said second switch and said second terminating resistor are also integrated into said single package.

13. The power amplifier of claim 1, wherein said first and said second power amplifiers constitute a balanced amplifier arrangement.

14. A power amplifier circuit arrangement, comprising:

a first switch which alternately switches an input signal between a bypass path and an amplifier path;

a driver stage positioned in said amplifier path and which receives said input signal and produces an amplified signal;

a first circuit element which receives said amplified signal and produces an in-phase signal and an out-of-phase signal;

a first power amplifier which receives and amplifies said in-phase signal;

a second power amplifier which receives and amplifies said out-of-phase signal;

a second switch which alternately connects an isolated port of said first circuit element to ground or said bypass path; and

a second circuit element which receives said amplified in-phase signal and said amplified out-of-phase signal and combines said in-phase and out-of-phase signals into an output signal, wherein an isolated port of said second circuit element is connected to ground.

15. The power amplifier arrangement of claim 14, wherein said first and said second power amplifiers are in a balanced amplifier arrangement.

16. The power amplifier circuit arrangement of claim 14, wherein when said driver stage is powered down, said first switch and said second switch connect said input signal to said bypass path in order to bypass said driver stage and inject said input signal to said first circuit element.

17. The power amplifier circuit arrangement of claim 14, further comprising a band-pass filter positioned between said first switch and said driver amplifier, said band-pass filter band-passing said input signal.

18. The power amplifier circuit of claim 14, wherein a bias and control circuit biases said driver stage, said first power amplifier and said second power amplifier, and said bias and control circuit controls said first switch and said second switch.

19. The power amplifier circuit of claim 14, wherein said first circuit element is a coupler and said second circuit element is a coupler, a first terminating resistor is connected to an isolated port of said second coupler, and a second terminating resistor is connected to a pole of said second switch.

20. The power amplifier circuit of claim 14, wherein said driver stage, said first circuit element, said second circuit element, said first amplifier, and said second amplifier are integrated into a single package.

21. The power amplifier circuit of claim 20, wherein said second switch and said second termination resistor are also integrated into said single package.

22. The power amplifier circuit of claim 19, wherein said first circuit element is a branch-line coupler and said second circuit element is a branch-line coupler.

23. A power amplifier circuit arrangement, comprising:

a first circuit element which receives an input signal and produces an in-phase signal and an out-of-phase signal, said first circuit element having a grounded isolated port;

a first power amplifier which receives and amplifies said in-phase signal;

a second power amplifier which receives and amplifies said out-of-phase signal;

a second circuit element which receives and combines said amplified in-phase signal and said amplified out-of-phase signal to produce an output signal;

a switch which alternately connects an isolated port of said second circuit element to ground or a signal distortion compensation path;

a signal processing circuit which receives a first coupled signal from said input signal and a second coupled signal from said output signal and produces a distortion compensation signal, wherein when said switch connects said isolated port of said second circuit element to said distortion compensation path, said distortion compensation signal being input to said isolated port of said second circuit element.

24. The power amplifier circuit of claim 23, further comprising a driver stage providing said input signal to said first circuit element.

25. The power amplifier circuit of claim 24, wherein a bias and control circuit biases said driver stage, said first power amplifier and said second power amplifier, and said bias and control circuit controls said switch.

26. The power amplifier circuit of claim 23, wherein said first circuit element is a coupler and said second circuit element is a coupler, and a first terminating resistor is connected to said isolated port of said first coupler.

27. The power amplifier circuit of claim 26, wherein a second terminating resistor is connected to a pole of said switch.

28. The power amplifier circuit of claim 23, wherein a third power amplifier amplifies said distortion compensation signal output from said signal processing circuit.

29. The power amplifier circuit of claim 23, where said first circuit element, said first power amplifier, said second power amplifier, said switch, and said second circuit element are integrated into a single package.

30. The power amplifier circuit of claim 25, where said first circuit element, said first power amplifier, said second power amplifier, said second circuit element, said switch, said driver stage, and said bias and control circuit are integrated into a single package.

31. The power amplifier circuit of claim 28, where said first circuit element, said first power amplifier, said second power amplifier, said second circuit element, said switch, and said third power amplifier are integrated into a single package.

32. (currently amended) In a power amplifier circuit arrangement comprising a first circuit element adapted receive an input signal and produce an in-phase signal and an out-of-phase

signal, a first power amplifier connected to a first output of said first circuit element, a second power amplifier connected to a second output of said first circuit element, a first switch alternately connecting an isolated port of said first circuit element between ground and a bypass path, a second circuit element having a first port connected to an output of said first power amplifier and a second port connected to an output of said second power amplifier, a second switch alternately connecting an isolated port of said second circuit element between ground and said bypass path, a method of bypassing said first and second power amplifiers comprising:

in a power amplifier bypass mode:

connecting said isolated port of said first circuit element to said bypass path using said first switch;

connecting said isolated port of said second circuit element to said bypass path using said second switch;

splitting said input signal into said in-phase signal and said out-of-phase signal using said first circuit element;

reflecting said in-phase signal off said first power amplifier;

reflecting said out-of-phase signal off said second power amplifier;

combining said reflected in-phase and said out-of-phase signals at said first circuit element;

transmitting said combined signal from said isolated port of said first circuit element through said bypass path to said isolated port of said second circuit element;

splitting said combined signal into a second in-phase signal and a second out-of-phase signal in said second circuit element;

reflecting said second in-phase signal off said second power amplifier in said second circuit element;

reflecting said second out-of-phase signal off said first power amplifier; and

combining said reflected second in-phase and said reflected out-of-phase signals at said second circuit element to produce a combined signal; and

in a power amplification mode:

connecting said isolated port of said first circuit element to ground by said first switch;

connecting said isolated port of said second circuit element to ground by said second switch;

splitting said input signal into said in-phase signal and said out-of-phase signal using said first circuit element;

amplifying said in-phase signal using said first power amplifier;

amplifying said out-of-phase signal using said second power amplifier; [and]

combining said amplified in-phase and said out-of-phase signals at said second circuit element to produce a combined output signal;

receiving said input signal and amplifying said input signal using a driver stage;

controlling said first switch and said second switch using a bias and control circuit; and

biasing said driver stage, said first amplifier, and said second amplifier using said bias and control circuit.

33. (cancel)

34. In a power amplifier circuit arrangement comprising a driver amplifier receiving an input signal and producing an amplified signal, a first circuit element which receives said amplified input signal and produces an in-phase signal and an out-of-phase signal, a first power amplifier connected to a first output of said first circuit element, a second power amplifier connected to a second output of said first circuit element, a first switch alternately routing said input signal to said driver amplifier or a bypass path, a second circuit element having a first port connected to an output of said first power amplifier and a second port connected to an output of said second power amplifier, said second circuit element having a grounded isolated port, a second switch alternately connecting an isolated port of said first circuit element between ground and said bypass path, a method of bypassing said driver amplifier comprising:

in a driver amplifier bypass mode:

routing said input signal to said bypass path using said first switch;

connecting said isolated port of said first circuit element to said bypass path via said second switch;

splitting said input signal into said in-phase signal and said out-of-phase signal using said first circuit element;

amplifying said in-phase signal using said first power amplifier and transmitting said amplified in-phase signal to said second circuit element;

amplifying said out-of-phase signal using said second power amplifier and transmitting said amplified out-of-phase signal to said second circuit element;

combining said amplified in-phase and said amplified out-of-phase signals at said second circuit element;

transmitting said combined signal to an RF-output port; and

in a power amplification mode:

routing said input signal to said driver amplifier by said first switch;

connecting said isolated port of said first circuit element to ground by said second switch;

splitting said input signal received from said driver amplifier into said in-phase signal and said out-of-phase signal using said first circuit element;

amplifying said in-phase signal using said first power amplifier and transmitting said amplified in-phase signal to said second circuit element;

amplifying said out-of-phase signal using said second power amplifier and transmitting said amplified out-of-phase signal to said second circuit element;

combining said amplified in-phase and said amplified out-of-phase signals at said second circuit element; and

transmitting said combined signal to an RF-output port.

35. The method of bypassing the driver amplifier of claim 31, further comprising:

controlling said first switch and said second switch using a bias and control circuit; and

biasing said driver stage, said first amplifier, and said second amplifier using said bias and control circuit.

36. In a power amplifier circuit arrangement, comprising a driver stage receiving an input signal and producing an amplified signal, a first circuit element which receives said amplified input signal and produces an in-phase signal and an out-of-phase signal, said first element having

a grounded isolated port, a first power amplifier connected to a first output of said first circuit element, a second power amplifier connected to a second output of said first circuit element, a second circuit element having a first port connected to an output of said first power amplifier and a second port connected to an output of said second power amplifier, said second circuit element having an isolated port and said second circuit element producing an output signal, a signal processing element which couples said input signal with said output signal and produces a distortion compensation signal in a distortion compensation path, a switch alternately connecting said isolated port of said second circuit element between ground and a distortion compensation path, a method of providing distortion compensation comprising:

coupling said signal processing element to said input signal and said output signal;

producing a distortion compensation signal corresponding to said input signal and said output signal, said distortion compensation signal generated to cancel distortion caused by said first and second amplifiers;

connecting said distortion compensation path from said signal processing element to said second circuit element using said switch;

inserting said distortion compensation signal into said second circuit element; and

canceling distortion within said input signal using said distortion compensation signal.

37. The method of bypassing the driver stage of claim 36, further comprising:

controlling said switch using a bias and control circuit; and

biasing said driver amplifier, said first amplifier, and said second amplifier using said bias and control circuit.

38. (cancel)